What is claimed is:

1. A method of forming a coupling dielectric in a memory cell comprising:

forming an oxide on a substrate;

forming $Ta_2O_5$ on the oxide;

oxidizing the $Ta_2O_5$ with rapid thermal process (RTP) at a temperature above the crystallization temperature for $Ta_2O_5$;

forming a cell nitride on the oxidized $Ta_2O_5$; and

forming a wetgate oxide on the cell nitride.

2. The method of claim 1, wherein oxidizing the $Ta_2O_5$ with rapid thermal process (RTP) at the temperature above the crystallization temperature for $Ta_2O_5$ comprises:

oxidizing the $Ta_2O_5$ with rapid thermal process (RTP) in $N_2O$ at a temperature of between about 750 degrees centigrade and about 900 degrees centigrade.

3. The method of claim 2, further comprising cooling for between about 55 seconds and about 65 seconds after oxidizing the $Ta_2O_5$.

4. A method of forming a coupling dielectric in a memory cell comprising:

forming an oxide on a substrate;

forming $Ta_2O_5$ on the oxide;

oxidizing the $Ta_2O_5$ with rapid thermal process (RTP) at a temperature below the crystallization temperature for $Ta_2O_5$;

forming a cell nitride on the oxidized $Ta_2O_5$; and

forming a wetgate oxide on the cell nitride.

5. The method of claim 4, wherein oxidizing the $Ta_2O_5$ with rapid thermal process (RTP) at the temperature below the crystallization temperature for $Ta_2O_5$ comprises:

oxidizing the $Ta_2O_5$ in rapid thermal process (RTP) in $N_2O$ at a temperature of between about 400 degrees centigrade and about 725 degrees centigrade.

6. The method of claim 5, further comprising cooling for between about 55 seconds and about 65 seconds after oxidizing the $Ta_2O_5$.

7. A method of forming a coupling capacitor in a memory cell comprising:

forming an oxide on a substrate to a depth of about 30 angstroms;

forming a tantalum oxide having a crystallization temperature on the oxide to a depth of between about 60 angstroms and about 100 angstroms;

oxidizing the tantalum oxide at a temperature above the crystallization temperature of tantalum oxide;

forming a cell nitride on the oxidized tantalum oxide to a depth of between about 40 angstroms and about 60 angstroms; and

forming a wetgate oxide to a depth of between about 10 angstroms and about 50 angstroms on the cell nitride.

8. The method of claim 7, wherein forming the tantalum oxide on the oxide to the depth of between about 60 angstroms and about 100 angstroms comprises:

forming $Ta_2O_5$ on the oxide to a depth of between about 60 angstroms and about 100 angstroms.

9. The method of claim 8, further comprising oxidizing the tantalum oxide in rapid thermal processing (RTP) in $N_2O$ for about 60 seconds.

10. A method of forming a coupling capacitor in a memory cell comprising:

forming an oxide on a substrate to a depth of about 30 angstroms;

forming a tantalum oxide having a crystallization temperature on the oxide to a depth of between about 60 and about 100 angstroms;

oxidizing the tantalum oxide at a temperature below the crystallization temperature of tantalum oxide;

forming a cell nitride on the oxidized tantalum oxide to a depth of between about

40 angstroms and about 60 angstroms; and

forming a wetgate oxide to a depth of between about 10 angstroms and about 50 angstroms on the cell nitride.

11. The method of claim 10, wherein forming the tantalum oxide on the oxide to the depth of between about 60 and about 100 angstroms comprises:

forming $Ta_2O_5$ on the oxide to a depth of between about 60 angstroms and about 100 angstroms.

12. The method of claim 11, further comprising oxidizing the tantalum oxide in rapid thermal processing (RTP) in $N_2O$ for about 60 seconds.

13. A method of forming a coupling dielectric in a memory cell comprising:

forming a layer of $SiO_2$ on a substrate;

forming a layer of $Ta_2O_5$ on the layer of $SiO_2$;

forming a layer of $Si_3N_4$ on the layer of $Ta_2O_5$; and

forming a layer of $SiO_2$ on the layer of $Si_3N_4$.

14. The method of claim 13, wherein forming the layer of $SiO_2$ on the substrate comprises forming the layer of $SiO_2$ on germanium.

15. The method of claim 14, wherein forming the layer of $Ta_2O_5$ on the layer of $SiO_2$ comprises oxidizing the tantalum layer above the crystallization temperature.

16. A method of forming a coupling dielectric in a memory cell, comprising:

forming an oxide layer on a substrate;

forming a tantalum oxide layer on the oxide layer;

forming a nitride layer on the tantalum oxide layer; and

forming a oxide layer on the nitride layer.

17. The method of claim 16, wherein forming the oxide layer on the substrate comprises forming the oxide layer on gallium arsenide.

18. The method of claim 16, wherein forming the tantalum oxide layer on the oxide layer comprises oxidizing the tantalum layer above the crystallization temperature.

19. A method of forming a coupling dielectric in a memory cell, comprising:

forming a thermally grown oxide layer having a thickness of between about 28 angstroms and about 32 angstroms on a substrate;

forming a tantalum oxide layer on the thermally grown oxide layer;

forming a nitride layer on the tantalum oxide layer; and

forming a oxide layer on the nitride layer.

20. The method of claim 19, wherein forming the thermally grown oxide layer having a thickness of between about 28 angstroms and about 32 angstroms on the substrate comprises forming the thermally grown oxide layer on a silicon-on-sapphire substrate.

21. The method of claim 19, wherein forming the tantalum oxide layer on the thermally grown oxide layer comprises reoxidizing the tantalum layer by rapid thermal processing.

22. A method of forming a coupling dielectric in a memory cell, comprising:

forming an oxide layer on a substrate;

forming a tantalum oxide layer by metal organic chemical vapor deposition to a thickness of between about 60 angstroms and about 100 angstroms on the oxide layer;

forming a nitride layer on the tantalum oxide layer; and

forming a oxide layer on the nitride layer.

23. The method of claim 22, wherein forming the oxide layer on the substrate comprises forming the oxide layer on an amorphous material.

24. The method of claim 22, wherein forming the oxide layer on the substrate comprises forming the oxide layer by chemical vapor deposition.

25. A method of forming a coupling dielectric in a memory cell, comprising:

forming an oxide layer on a substrate;

forming a layer of a material having a permittivity of between about ten and about twelve on the oxide layer;

forming a nitride layer on the tantalum oxide layer; and

forming a oxide layer on the nitride layer.

26. The method of claim 25, wherein forming the oxide layer on the substrate comprises forming the oxide layer on a n+ substrate.

27. The method of claim 25, wherein forming the oxide layer on the substrate comprises forming the oxide layer by chemical vapor deposition.

28. A method of forming a coupling dielectric in a memory cell, comprising:

forming an oxide layer on a substrate;

forming a tantalum oxide layer on the oxide layer;

forming a nitride layer having a thickness of between about 40 angstroms and about 60 angstroms on the tantalum oxide layer; and

forming a oxide layer on the nitride layer.

29. The method of claim 28, wherein forming the oxide layer on the substrate comprises forming the oxide layer on a germanium substrate.

30. The method of claim 28, whereon forming the nitride layer having the thickness of between about 40 angstroms and about 60 angstroms on the tantalum oxide layer comprises forming the nitride layer by low pressure chemical vapor deposition.

31. A method of forming a coupling dielectric in a memory cell, comprising:

forming an oxide layer on a substrate;

forming a tantalum oxide layer on the oxide layer;

forming a nitride layer on the tantalum oxide layer; and

forming a oxide layer having a thickness of between about 10 angstroms and about 50 angstroms on the nitride layer.

32. The method of claim 31, wherein forming the oxide layer on the substrate comprises forming the oxide layer on a silicon substrate.

33. The method of claim 31, wherein forming the oxide layer on the substrate comprises forming the oxide layer on a gallium arsenide substrate.